Novel Microelectronic Packaging Method for Reduced Thermomechanical Stresses on Low Dielectric Constant Materials

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ABSTRACT

Incorporation of fragile, low dielectric constant (low *k*) materials into the back end interconnect structures of silicon devices requires a packaging method that minimizes stresses induced on these structures. We propose a new package, called a Bumpless Build Up Layer (BBUL) package, which addresses this challenge. The package architecture differs from traditional assembled packages in that it consists of a die or dice embedded in a substrate, which then has one or more build up layers formed on top. This work discusses the overall structure of the BBUL package and compares relative thermomechanical impacts of BBUL versus flip chip packages on low *k* interlayer dielectric layers integrated on the die.

INTRODUCTION

One of the main challenges for future generations of logic technology is the integration of low dielectric constant (low *k*) materials on-chip. Low *k* materials ($k \approx$ 2-3) tend to have poor mechanical robustness. During temperature excursions, mismatch of the coefficients of thermal expansion (CTE) among the various component materials of a package can cause fatal stresses in such structures at the active die surface.

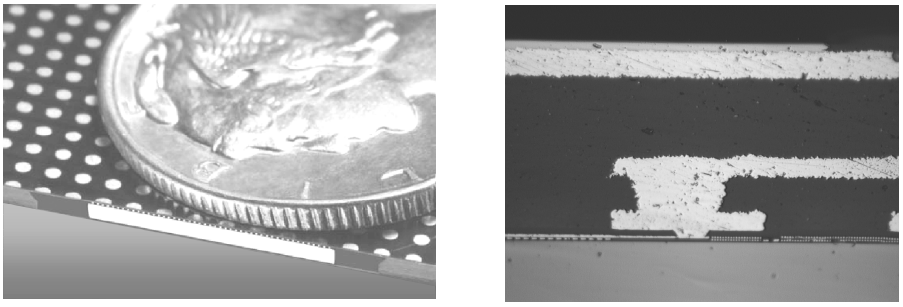
We have developed a package that potentially addresses this challenge, the Bumpless Build Up Layer (BBUL) package. BBUL is designed to meet packaging technology requirements for Intel's 65 nm generation silicon technology and beyond. In this paper we discuss the process for making a BBUL package, and, through finite element simulations, demonstrate the mechanical advantages provided by BBUL in terms of its compatibility with the use of low *k* materials on die. The numerical results are compared to a simulation of a flip chip package with an organic land grid array (OLGA) substrate and lead-tin (high lead content) bumps. This package type has been used by Intel for packaging microprocessors for some years, and is considered to have good mechanical performance due to the low yield strength, and therefore high compliance, of the high-lead bumps.

Besides the mechanical advantages, the BBUL structure provides enhancements in several other areas. This package provides the advantages of low loop inductance for decoupling capacitors, high lead count, ready integration of multiple electronic and optical components [*e.g.*, logic, memory, radio frequency, microelectromechanical systems (MEMS), *etc.*], and inherent scalability. These advantages, including results of simulations showing a significant improvement in electrical power delivery performance for BBUL when compared to a standard FCPGA package, are presented elsewhere [1].

PACKAGE FABRICATION

BBUL differs from traditional assembled packages in that it consists of a die (or dice) embedded in a substrate, which then has one or more build-up layers formed on top. The die may be embedded in the panel by molding or with dispensed encapsulation material. As shown in Figure 1(b), the die surface is terminated with copper pads that cover the normal bond pad openings and act as landing pads for the laser drilling process. The first build up dielectric layer

is deposited on the die-embedded substrate, then laser drilling forms the microvias. Build up layers are formed sequentially by a standard high-density interconnect (HDI) patterning process. The structure is analogous to a wafer level CSP (WLCSP), but with the die embedded in the panel to increase the available fan out area and with the possibility of multiple wiring layers. The build-up technology is similar to what is typically used for advanced organic packages (e.g., Intel's FCPGA package). Further details of the fabrication process are discussed elsewhere [1]. The package is shown in Figure 1a (without a heat lid).



(a) (b)

Figure 1. Views of a BBUL package: (a) photo of a portion of the BBUL package without heat lid, showing the die (white) and a dime for scale; (b) cross-sectional SEM image of build-up layers at the surface of the die (at bottom).

MODELING PROCEDURES

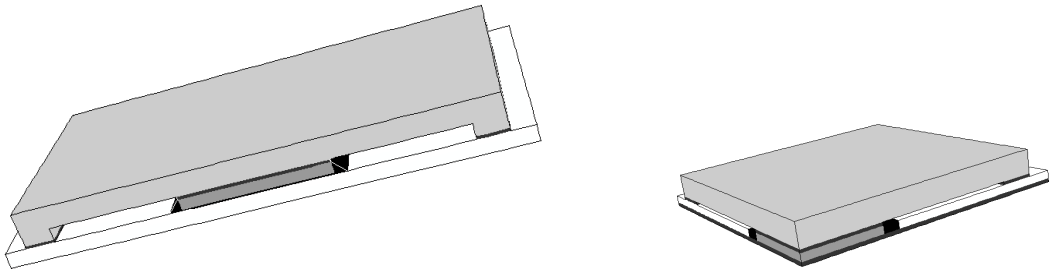
In order to investigate the thermomechanical performance of the BBUL package, a finite element simulation of this package was performed through one temperature excursion (150 °C to –55 °C). These results are compared to a simulation of a flip chip package subjected to the same conditions. Since the BBUL package places only thin layers in contact with the die surface, the pad geometry may be expected to contribute significantly to the local stress state at the die surface. Thus, BBUL was examined with two landing pad thicknesses: 10 μm and 3 μm.

To measure the mechanical performance, we assessed thermomechanical effects leading to interlayer dielectric (ILD) cracking, delamination from surrounding layers, and shape distortion. The failures seen in on-chip interconnect are dependent on, among other factors, the mechanical properties of the dielectric material. Here we have assumed the ILD to be a brittle doped-oxide dielectric such as is described in [2]. On a larger scale, the general package deformation was examined.

The mechanical modeling was performed using the commercial finite element code ABAQUS™. We used global/local modeling to examine the effect of the package on these structures. In this procedure, a "global" model captures the overall deformation of the entire package. The displacements in a specific region of the model are then used as boundary conditions for the "local" model, which examines a smaller area in greater detail. For the present case, we have three levels of hierarchy in the modeling: global, regional, and local.

The geometries of the flip chip and BBUL global models are shown in Figure 2. The models are half- and quarter-symmetric, respectively. Common elements of both models are a 10 mm × 10 mm × 725 μm polysilicon die (medium gray), a 34 mm × 34 mm × 725 μm bismaleimide triazine (BT) laminate substrate/core (white), 200 μm thick indium thermal interface material between the die and heat lid, 200 μm thick silicone rubber heat lid sealant adhering the heat lid to the substrate/core, and a 31 mm × 31 mm × 1.5 mm copper heat lid (light gray). For the flip chip model, epoxy underfill and 90%Pb-10%Sn solder joints form the bond between the substrate and

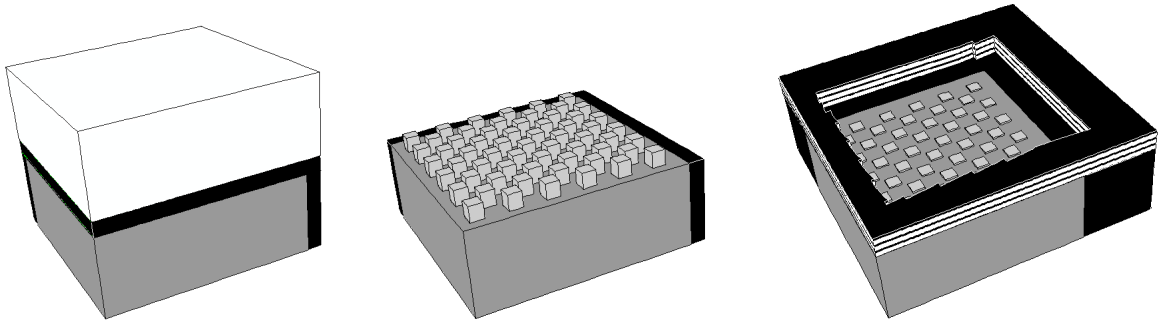
die (black), with a 90 μm bump height. For BBUL, the die with Cu landing pads is embedded in the core with 1 mm wide epoxy encapsulant (black). As mentioned, two cases were examined: pad heights of 10 μm and 3 μm (referred to as 10μm-BBUL and 3μm-BBUL, respectively). Finally, on the underside of the BBUL model in Figure 1 are the build-up layers (dark gray). The build-up layers are three alternating layers of an epoxy build up dielectric material (30 μm thickness) and copper (15 μm); they are included as solid planes without lines or vias.



(a) (b)

Figure 2. Geometries of (a) flip chip and (b) BBUL models. Flip-chip was modeled as half-symmetric, BBUL as quarter-symmetric.

The flip chip regional model is shown both in its entirety (Figure 3a), and again with the substrate and underfill removed (Figure 3b) to reveal details of the bump array. The regional BBUL model is shown in Figure 3c, with a portion of the build-up layers removed to reveal the pads on the die. Both models consist of the die corner (medium gray) and surrounding epoxy (black), and bumps or pads (light gray). Specific to the flip chip model are the underfill (black), and substrate (white); BBUL-specific is the build up, which is alternating layers of modified ABF and copper (white and black, respectively). The bumps/pads are aligned in a face-centered pattern with a pitch of 150 μm. The flip chip bump size is 80 μm × 80μm × 90 μm. The BBUL pads are 80 μm × 80 μm × *t*, where *t* was set to either 10 μm or 3 μm, as mentioned above.

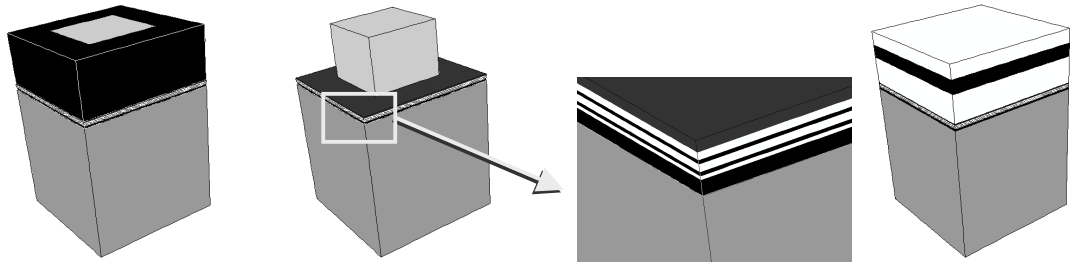


(a) (b) (c)

Figure 3. Regional models: (a) the flip chip package model shown in its entirety; (b) with substrate and underfill removed to reveal the bump array on the die surface; (c) the BBUL package with a portion of the build-up removed to the reveal pad array on the die surface.

The flip chip and BBUL local models are shown in Figure 4. The local models consist of the area immediately surrounding the bump or pad nearest the corner of the die, and extend in the thickness direction from inside the silicon to about 60 μm above the die surface. The ILD stack (Figure 4c) includes (moving towards the die): passivation (dark gray), the "M3" copper layer (white), the "V2" ILD layer (black), the M2 copper layer (white), the V1 ILD layer (black), the M1 copper layer (white), and a final ILD layer, V0 (black). All analyses were non-linear quasi-static; no rate effects of any of the materials have been included. All of the structures were con-

sidered stress-free at 150 °C, and then uniformly cooled to –55 °C. All of the models used 20-node quadratic hexahedral elements, except for the flip chip global model, which used 8-node linear hexahedrals.



(a) (b) (c) (d)

Figure 4. Local model of flip chip package (a) in its entirety and (b) with underfill removed to reveal the solder bump. (c) Detailed view of the ILD stack on the die surface. (d) Local model of BBUL package.

FAILURE THEORY

When the first principal stress (σ_1) in a stressed body is greater than zero, it represents the greatest tensile stress present in the body (at a point). If one assumes the presence of many small flaws randomly oriented in a material, this maximum tension has the highest probability of causing Mode I fracture, the most common mode of failure [3]. Thus, for brittle materials, the likelihood of cracking is correlated to the magnitude of σ_1 in a material, provided it is greater than zero [4]. When considering interfacial failure, if one assumes flaws to lie along the interface, then the above arguments apply but with the crack opening stress constrained to be normal to the interface. The Von Mises effective stress (σ_M) in a body is related to the distortional energy of that body. This is considered a good indicator of failure for materials that deform plastically, where failure is considered to occur when a part becomes distorted beyond a certain amount [4].

MODELING RESULTS

Figure 5 shows contours of displacement in the 3-direction (u_3) for the flip chip (left) and BBUL (right) packages, as measured on the land side of the package. The coordinate axes are as shown in the figure; this model orientation was maintained throughout all of the models discussed here. For the flip chip package, u_3 reaches a minimum between the die center and package edge. The total amplitude of this displacement is roughly 50 μm. For BBUL, the vertical displacement is monotonically increasing when moving from die center to package edge; the maximum amplitude of this displacement is about 40 μm. These displacements are shown for the 10μm-BBUL package only, but the 3μm-BBUL showed no noticeable difference.

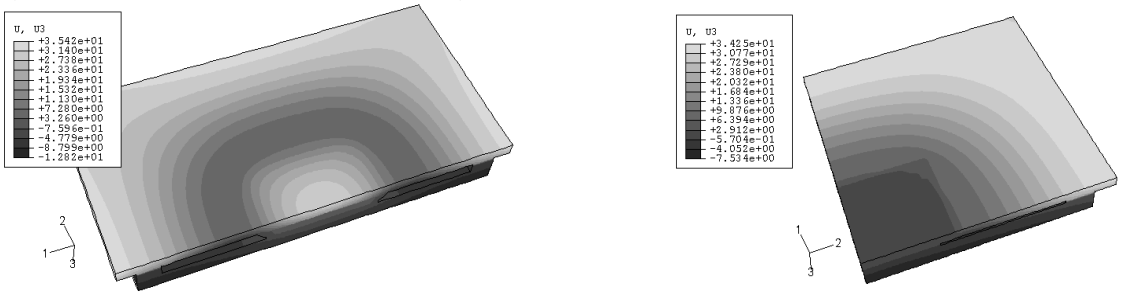
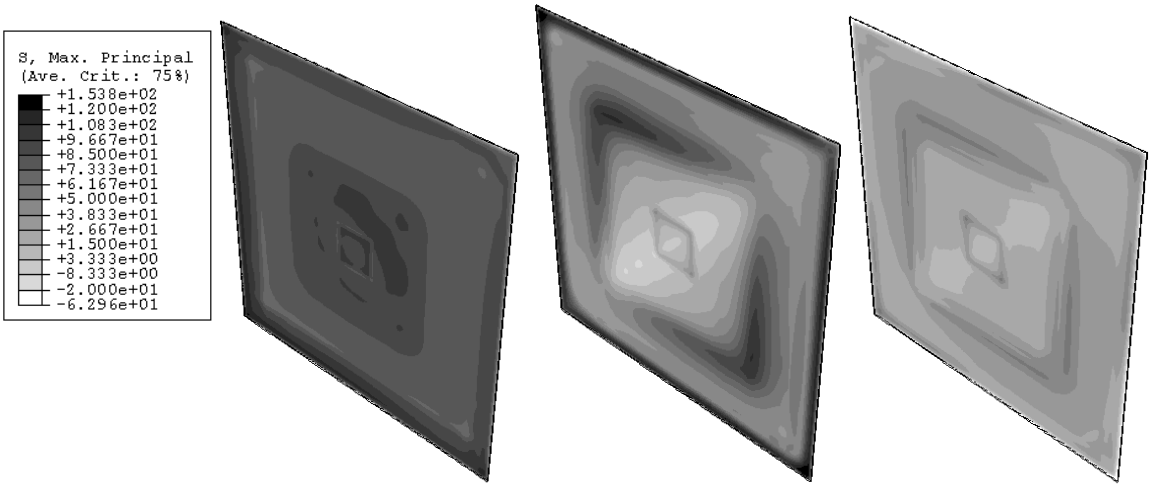


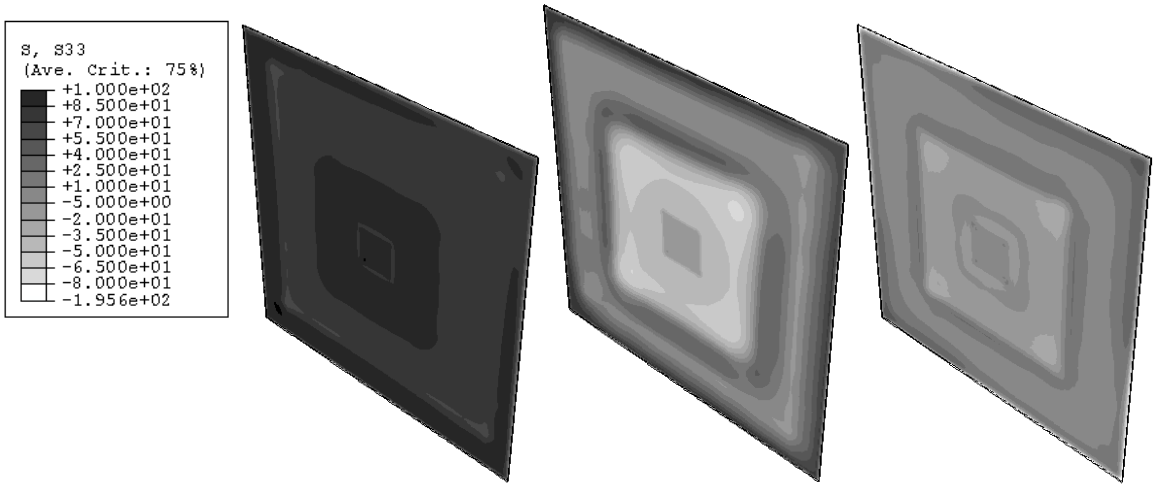
Figure 5. Vertical displacement (in μm) on the land side of the flip chip (left) and BBUL (right) packages.

The first principal stress in the V2 layer between metal layers M2 and M3 is shown in Figure 6 for (a) the flip chip package, (b) 10μm-BBUL, and (c) 3μm-BBUL. The stress plots are shown as a slice through the V2 level of the local model in Fig. 4(c), rotated in space for clarity. When interpreting the local models care must be taken when considering areas near the edges of the model where the displacements from the global models are interpolated and imposed on the local models. In this discussion, the stress field very close to the edge of the model (within ~10 μm) will generally be ignored. The maximum principal stress away from the edges is similar for the flip chip and 10μm-BBUL, although the average principal stress is lower in the 10μm-BBUL case. The 3μm-BBUL package results in a lower first principal stress in this layer, by about a factor of two in the highest regions. Much of the layer has a first principal stress close to zero.



(a) (b) (c)

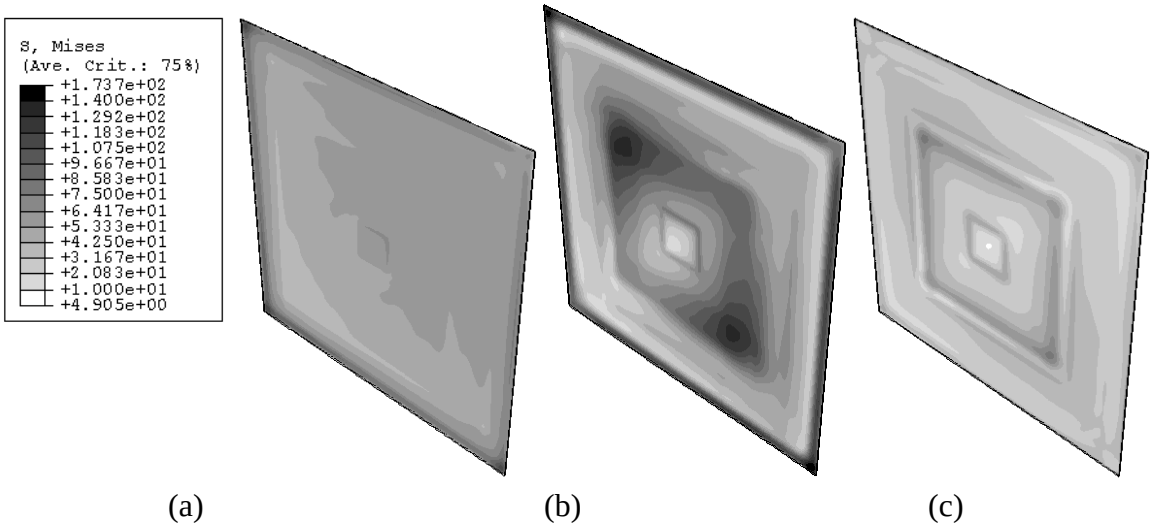
Figure 6. Contour plot of first principal stress (σ_1) in the V2 ILD layer for (a) flip chip package, (b) 10μm-BBUL, and (c) 3μm-BBUL. Stress scale ranges from -20MPa to 120MPa.



(a) (b) (c)

Figure 7. Contour plot of layer normal stress (σ_{33}) in theV2 ILD layer for (a) flip chip package, (b) 10μm-BBUL, and (c) 3μm-BBUL. Stress scale ranges from -80MPa to 100MPa.

The σ_{33} in the V2 layer (3-direction normal to layer) is shown in Figure 7 for the three packages. This stress is significantly higher for the flip chip package than for either of the BBUL cases. There are some areas of significant compression in the 10μm-BBUL case; these are not present for the 3μm-BBUL, for which σ_{33} is close to zero throughout the region. Figure 8 shows contours of σ_M in the V2 layer for the three packages. While the flip chip package induces a small σ_M throughout the layer in this region near the die corner, 10μm-BBUL has areas near the pad corners where the maximum σ_M is twice that for flip chip. Preliminary results show that changing the pad shape from square to round has a minimal affect on the magnitude of σ_M. On the other hand, for 3μm-BBUL, σ_M has a maximum value similar to that for the flip chip package, and apart from the pad corners was lower over the entire layer.



(a) (b) (c)

Figure 8. Contour plot of Von Mises effective stress in the V2 ILD layer for (a) flip chip package, (b) 10μm-BBUL, and (c) 3μm-BBUL. Stress scale ranges from 10MPa to 140MPa.

DISCUSSION

The two packages considered here showed different types of deformation, as seen from Figure 5. The flip chip package has a substrate that is constrained by two stiff entities, a silicon die and a copper heat lid. This causes the substrate to deform mostly in the areas where it is bonded to neither, creating relatively strong curvature in the region between the die edge and the heat lid seal. This could make board attachment difficult. BBUL does not have this problem, but instead has moderate vertical displacement from center to edge.

The maximum first principal stress was similar for 10μm-BBUL and flip chip, although the average was higher for flip chip. This leads us to believe that the probability of 10μm-BBUL causing crack opening is roughly similar to that for flip chip. For the 3μm-BBUL, the first principal stress was considerably smaller than for either of the other two cases, and presents the smallest probability of causing ILD cracking.

The out-of-plane tension in the ILD was lower for 10μm-BBUL than for flip chip, implying a lower risk of delamination in the ILD stack for BBUL. 10μm-BBUL showed some areas of significant out-of-plane compressive stress; this may be less likely to cause failure as brittle materials are relatively stable in compression. The magnitude of the maximum compression was smaller than the magnitude of maximum tension in the flip chip case. Again, 3μm-BBUL was

the best case, inducing stresses relatively close to zero in the ILD, as well as eliminating the high compressive stresses seen in the 10μm-BBUL.

We did find that the maximum σ_M in the 10μm-BBUL package was roughly twice that in the flip chip. This seems to be due to relatively larger shear stresses generated near the edges of the pad in the BBUL case. While this may not be an important indicator of failure in stiff, brittle materials, it could signify a problem when considering the use of a soft, ductile ILD material. However, 3μm-BBUL did not exhibit this problem, with σ_M generally lower than for the other packages examined, and in isolated areas a maximum stress similar to that for flip chip.

Generally, it was seen that changing the BBUL pad geometry had a strong effect on ILD stresses. This was apparently due to the relatively high compliance of the build up layers, making the pad the main contributor to ILD stress. This indicates that changes in the pad size, shape, and material may provide opportunities for further reduction in ILD stresses.

There are several features of the models that differ from the physical situation. The most notable is the assumption that all of the components start in a stress-free condition at 150 °C. In fact, the stress-free temperatures will differ from material to material throughout the die and package, depending on their process histories. Therefore, the magnitudes of the modeled stresses will in general differ from reality. However, it is expected that the trends discussed here will be preserved in actual packages, as the maximum temperatures in BBUL build up processing are similar to those for standard assembly processing presently done at Intel.

CONCLUSIONS

BBUL, a novel packaging technique, has been described, including its design and fabrication process. Numerical simulations have shown that this package will impose smaller stresses on structures at the die surface than a flip chip package with high-lead bumps, making it better suited for packaging microelectronic chips with fragile low *k* materials in the interconnect layers.

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